AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A recording pulse generator comprising:

a first delay line having plural circuit elements cascaded in multiple stages, wherein the first delay line;

~~a means that generates~~ outputs plural output ~~fine~~ clocks each having different phase differences with a clock inputted to the first stage of the first delay line, according to the number of stages of the plural circuit elements thereof;

a level shift stage that shifts the levels of the plural output clocks to generate plural fine clocks, respectively;

a selector ~~means~~ that selects an arbitrary fine clock ~~form~~ from the plural fine clocks generated; and

a recording pulse ~~generation means~~ generator that generates a recording pulse on the basis of a fine clock selected.

2. (currently amended): A recording pulse generator as claimed in Claim 1, further comprising a PLL oscillator that possesses an oscillator with plural circuit elements cascaded in multiple stages, compares the phase of a signal generated by the oscillator with the phase of the clock inputted to the first stage of the first delay line, and controls a voltage of a power supply line for the first delay line and the oscillator of the PLL oscillators according to the phase comparison result~~, wherein:~~

~~the first delay line is connected to the common power supply line with the oscillator, and the circuits elements of the first delay line are equivalent to the circuit elements of the oscillator~~.

3. (previously presented): A recording pulse generator as claimed in Claim 1, wherein the clock inputted to the first stage of the first delay line is an EFM clock that varies according to a recording speed.

4. (currently amended): A recording pulse generator as claimed in Claim 1, wherein the ~~clock selection means~~ selector is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks.

5. (currently amended): A recording pulse generator as claimed in Claim 1, wherein the recording pulse ~~generation means~~ generator is provided with a flip-flop circuit that operates based on a delayed clock selected by ~~the~~ a multiplexer.

6. (previously presented): A recording pulse generator as claimed in Claim 2, wherein the clock inputted to the first stage of the first delay line is an EFM clock that varies according to a recording speed.

7. (currently amended): A recording pulse generator as claimed in Claim 2 , wherein the ~~clock selection means~~ selector is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks.

8. (currently amended): A recording pulse generator as claimed in Claim 3, wherein the ~~clock selection means~~ selector is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks.

9. (currently amended): A recording pulse generator as claimed in Claim 6, wherein the ~~clock selection means~~ selector is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks.

10. (currently amended): A recording pulse generator as claimed in Claim 2, wherein the recording pulse ~~generation means~~ generator is provided with a flip-flop circuit that operates based on a delayed clock selected by ~~the~~ a multiplexer.

11. (currently amended): A recording pulse generator as claimed in Claim 3, wherein the recording pulse ~~generation means~~ generator is provided with a flip-flop circuit that operates based on a delayed clock selected by ~~the~~ a multiplexer.

12. (previously presented): A recording pulse generator as claimed in Claim 4, wherein the recording pulse ~~generation means~~ generator is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

13. (currently amended): A recording pulse generator as claimed in Claim 6, wherein the recording pulse ~~generation means~~ generator is provided with a flip-flop circuit that operates based on a delayed clock selected by ~~the~~ a multiplexer.

14. (currently amended): A recording pulse generator as claimed in Claim 7, wherein the recording pulse ~~generation means~~ generator is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

15. (currently amended): A recording pulse generator as claimed in Claim 8, wherein the recording pulse ~~generation means~~ generator is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.

16. (currently amended): A recording pulse generator as claimed in Claim 9, wherein the recording pulse ~~generation means~~ generator is provided with a flip-flop circuit that operates based on a delayed clock selected by the multiplexer.